Processor-in-the-Loop Validation of an Observer Current-based Dead-Beat Control for a Single-Phase UPS Inverter

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ABSTRACT

This paper presents a dead-beat control algorithm for Uninterruptible Power Supply (UPS) applications of single-phase inverters. The proposed control method requires the measurement of capacitor current and output voltage in order to keep the output voltage sinusoidal ensuring high dynamic performance even under load changes. The dead-beat controller optimizes the behavior of the system by eliminating the error between the output and the reference voltage without increasing the number of current sensors, which are costly, and eliminates load voltage distortions and restores the system state in the event of external shutdown-loop road interference. In this paper, we propose a capacitor current estimation based on the Luenberger observer. Processor-In-the-Loop (PIL) is a test method that allows us to create and evaluate controllers by running built-in C code on the DSP scheduled for the controller during simulated PSIM power phase control. It can be seen that the simulation results match the PIL test results, which proves the validity of the proposed controller.

Keywords-dead-beat control; single-phase inverter; PWM; Luenberger observer; PIL; DSP; CCS

I. INTRODUCTION

Using the output LC filter to control the inverters is important in applications such as distributed generation, renewable energy-based island applications, and Uninterruptible Power Supplies (UPSs) [1-3], where high quality voltage is required. The main control objective of UPS is to adjust the output voltage in the presence of parameter uncertainty and disturbance, and its characteristics depend on the quality of the output voltage. Disturbances from various loads, uncertainty due to inductive loads, non-linear loads, and model mismatches can lead to poor output voltage tracking and high Total Harmonic Distortion (THD). The effects of noise and uncertainty must be minimized to achieve excellent voltage performance. Any UPS system has two operating modes: backup mode and bypass mode. Ideally, a UPS should be able to deliver a regulated sinusoidal output voltage with low THD during the two modes and includes a dead-beat controller [4-10]. In [6, 11], the dead-beat controller is used with the disturbance observer for proper response and robust controlled performance. In [12-14], the PWM technique using a modified dead-beat controller is explained clearly, but the PWM pattern in the presence of load uncertainty is not detailed. In [15], the dead-beat control for power converters using fractional-order time delay compensation is defined as an effective and powerful delay compensation approach that has been applied in various control systems. In [16-21], single-phase inverter's deadbeat-based Proportional-Integral (PI) controller was proposed and comparisons with conventional control techniques were made. However, the implementation of the deadbeat controller is very complicated, and due to the

difficulty of its design, it is not suited for low cost implementations. However, the technique uses relatively higher energy losses.

The main purpose of control is to obtain a nearly sinusoidal output voltage across the output capacitor of the LC filter. Dead-beat control is the most attractive control method in discrete time systems because it can reduce the error between the reference and measured values as long as the number of samples goes to infinity and the error goes to zero, giving the inverter a fast dynamic response. The inverter's output voltage is achieved with very low THD. Dead-beat control is sensitive to variations of the filter parameters, even when the load fluctuates. The proposed dead-beat control system can work stably when the load variation is within the allowable range. In order to decrease the number of sensors, an observer to estimate the capacitor current is proposed. However, conventional dead-beat controllers suffer from two delays, the first is inherent to the dead-beat control algorithm and causes a steady-state error [12], and the second arises when the PSIM simulates the algorithm after CCS builds it and installs it on a DSP-based platform. It has an impact on the system's stability and causes ripples and phase shifts in the output current. The dead-beat response has some advantages:

- Zero steady-state error.
- Shortest rise time.
- Minimum settling period.
- An over/undershoot of less than 2%.
- Very high control signal output [16].

II. SYSTEM DESCRIPTION

The proposed single-phase inverter is shown in Figure 1 and consists of an H-bridge inverter connected to the load through LC filtering. Insulated Gate Bipolar Transistors (IGBTs) are chosen as the switching elements to perform energy transfer and power conversion. LC filters are used to filter higher harmonics before the load. The capacitor voltage and current are generated by the Luenberger observer. This system performs better with imbalanced loads and is more adaptable when it comes to working conditions.

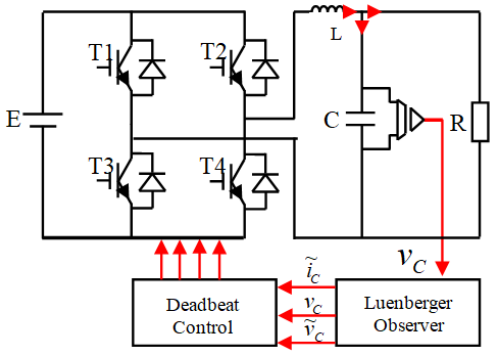


Fig. 1. Basic scheme of the proposed system.

III. THE CONSIDERED SYSTEM

The single-phase inverter consists of two arms in a half-bridge. If the power switches S1 and S'1 are supposed to be perfect (and are negligible), the system (source-inverter-filter-charge) is then represented by the second-order linear model of Figure 2.

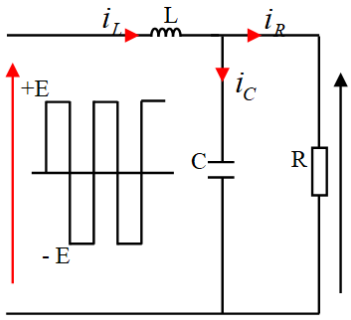


Fig. 2. Basic scheme of the proposed system.

This system's representation in state space is given by:

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{1}$$

where $x(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix}$. $x(t)$ is the state vector, such that:

$$\begin{cases} x_1(t) = v_c(t) \\ x_2(t) = \dot{v}_c(t) \end{cases} \tag{2}$$

According to the second-order linear model of the half-bridge inverter, applying the laws of Kirchhoff and calculating the matrices A and B, we get:

$$v_{\text{int}}(t) = v_L(t) + v_C(t) \tag{3}$$

$$v_{\text{int}}(t) = LC\,\ddot{v}_C(t) + \frac{L}{R}\dot{v}_C(t) + v_C(t) \tag{4}$$

By (4) we have:

$$\begin{cases} \dot{x}_1(t) = x_2(t) \\ \dot{x}_2(t) = \ddot{v}_C(t) = \dfrac{1}{LC}v_{\text{int}}(t) + \dfrac{1}{RC}x_2(t) - \dfrac{1}{LC}x_1(t) \end{cases} \tag{5}$$

So:

$$A = \begin{pmatrix} 0 & 1 \\ \dfrac{1}{LC} & \dfrac{1}{RC} \end{pmatrix} \text{ and } B = \begin{pmatrix} 0 \\ \dfrac{1}{LC} \end{pmatrix}.$$

Figure 3 shows the waveforms of $V_{inv}(t)$ during a sampling period T_e, where V_{inv} is the output voltage of the inverter and has two values, $+E$ and $-E$.

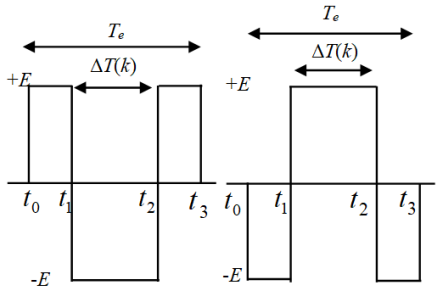


Fig. 3. Two-level PWM pattern.

The discrete-time system equation of the two-lever switching patterns is [14]:

$$x(t) = \exp\left[A(t-t_0)\right]x(t_0) + \int \exp\left[A(t-\tau)\right]B\,v_{\text{int}}(\tau)\,d\tau \quad (6)$$

Thus, the discrete state equation from t_0 to $t_1$and t_2 to t_3 is:

$$X[(k+1)\,T_e] = \exp\left[A\,T_e\right]X(k) + \exp\left[A\frac{T_e}{2}\right]BE\Delta T(k),\ E\Delta T(k) = v_{\text{int}}(\tau) \quad (7)$$

We will find from (8) the value of the duration ΔT that we must apply at all times to generate the control signals of the switches. $\Delta T(k)$ equals to the pulse-width in the k^{th} sampling interval. Assuming $T \ll 2\pi\sqrt{LC}$, the exponential quantities in (7) are approximated using the power series expansion:

$$A_k = \exp[AT] = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix}$$

$$A_k = \begin{bmatrix} 1-\frac{T^2}{2LC} & T-\frac{T^2}{2RC} \\ \frac{-1}{LC}+\frac{T^2}{2RLC^2} & 1-\frac{T}{RC}+(\frac{1}{R^2C^2}+\frac{1}{LC})\frac{T^2}{2} \end{bmatrix} \quad (8)$$

In order to improve this problem, a predictive dead-beat control method is proposed, in which the control input at the k^{th} sampling time is predicted by using the system values at the $(k\text{-}1)^{\text{th}}$ sampling time. PWM modulation signal, i.e. the reference output voltage of the inverter, calculated by the reference voltage V_{ref}, the actual capacitor current i_C, and the output load voltage of the inverter V_{ch} at the $(k\text{-}1)^{\text{th}}$ sampling time calculated with the reference voltage can be described as:

$$X(k+1) = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} X(k) + \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} E\Delta T(k) \quad (9)$$

The first line of (9) gives us the recurrent expression of the sampled output voltage:

$$\Delta T = \frac{1}{g_1 E}(V_{ref}(k+1) - \phi_{11}x_1 - \phi_{12}x_2) \quad (10)$$

IV. STATE OBSERVER

In the control system, observers can replace sensors. We can't estimate the state variables for which the observer is utilized. For the proposed control, capacitor current measurement is necessary and the principle of the observer is combining the feedback signal measured with the known components of the control system. The plant's behavior may be predicted with more precision than when the feedback signal is used alone. The observer augments the sensor output and provides a feedback signal to the control laws, as shown in Figure 4.

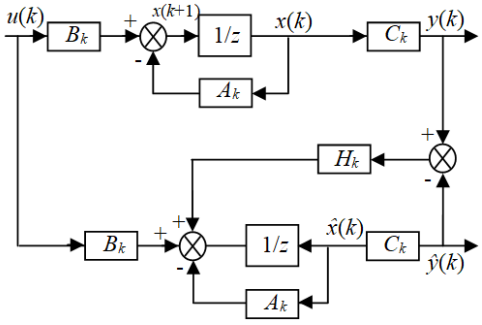


Fig. 4. Diagram of an observer.

A. Designing the State Observer

To introduce an observer to the system presented by (9), the system must be observable. For a system to be observable, it is sufficient that the size of the rows of the observability matrix O is equal to the number of state variables *n*. Hence the observability matrix is:

$$O = \begin{pmatrix} C \\ CA \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ \phi_{11} & \phi_{12} \end{pmatrix} \quad (11)$$

$Rang\,(O) = 2 = n$, verified condition.

B. The Observer Model

The state representation for a linear discrete system is:

$$SYS = \begin{cases} x(k+1) = A_k\,x(k) + B_k\,u(k) \\ y(k) = C_k\,x(k) \end{cases} \quad (12)$$

where $A_k = \begin{pmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{pmatrix}$, $B_k = \begin{pmatrix} g_1 \\ g_2 \end{pmatrix}$, $C_k = \begin{pmatrix} 1 & 0 \end{pmatrix}$.

The state vector of the system $x(k)$, is reconstructed using an observer whose dynamic equation, based on Luenberger's method, is expressed as:

$$\hat{x}(k+1) = A_k\,\hat{x}(k) + B_k\,u(k) + H_k\,(y(k) - \hat{y}(k)) \quad (13)$$
$$\hat{y}(k) = C_k\,\hat{x}(k)$$

where $u(k)$ is defined as input, $\hat{y}(k)$ is the estimated output, H_k is the observer's gain, and $\hat{x}(k)$ is the estimated state vector.

The error $e(k)=x(k)-\hat{x}(k)$ must converge to zero for all values of k for the observer to be stable. When the observer error satisfies the equation $e(k+1)=(A_k-H_k.C_k)e(k)$, then $(A_k-H_k.C_k)$ has its eigenvalue λ_i inside the unit circle. The determination of this matrix means that $|\lambda_{i=1....n}|<1$.

The choice of the eigenvalues must be such that the module is lower than 1 in order to ensure stability, the real part is closer to $z = 0$ to ensure a faster real part, and the imaginary part is faster if the angle to the real axis increases, but it should not be very close to the unit circle because otherwise the pole will be more resonant. Therefore λ_1 and λ_2 are chosen as:

$$\begin{cases}\lambda_1=0.1+j0.1\\ \lambda_2=0.1-j0.1\end{cases} \quad (14)$$

By calculating the determinant of the matrix $(zI-A_k+H_kC_k)$ and by identification on the polynomial $(z-\lambda_1)(z-\lambda_2)$ we can find h_1 and h_2:

$$\det(zI-A_k+H_kC_k)=(z-\lambda_1)(z-\lambda_2) \quad (15)$$

The components of H_k are given by:

$$\begin{cases}h_1=\phi_{11}+\phi_{22}-\lambda_1-\lambda_2\\ h_2=\dfrac{1}{\phi_{12}}\left[\lambda_1\lambda_2+\phi_{22}(\phi_{22}-\lambda_1-\lambda_2)\right]+\phi_{21}\end{cases} \quad (16)$$

V. SIMULATION STUDY

Simulations and tests can be used to determine the performance of the above suggested control technique using the DSP F28335 to implant the control algorithm in the digital circuit and IGBT switching devices for the single phase inverter. The inverter's switching frequency is set to 10kHz, and the algorithm's sample period is set to 0.0001s. The inverter's design parameters are given in Table I.

TABLE I. PARAMETERS OF THE INVERTER

Parameter	Value
Rated output voltage *Vc*	220V
DC link voltage *E*	400V
Filter inductance *L*	2mH
Resistance *R*	20Ω
Filter capacitor *C*	20uF
Sampling frequency *Fs*	10kHz

The system's simulation results are presented with and without the presence of the observer, in order to show the role played by the latter in replenishing the V_C voltage as well as to ensure a good release of the disturbance when connecting charges occur.

VI. PIL IMPLEMENTATION

The DSP is connected to the computer with a USB cable, which is the hardware configuration required for PIL simulation as shown in Figure 9.

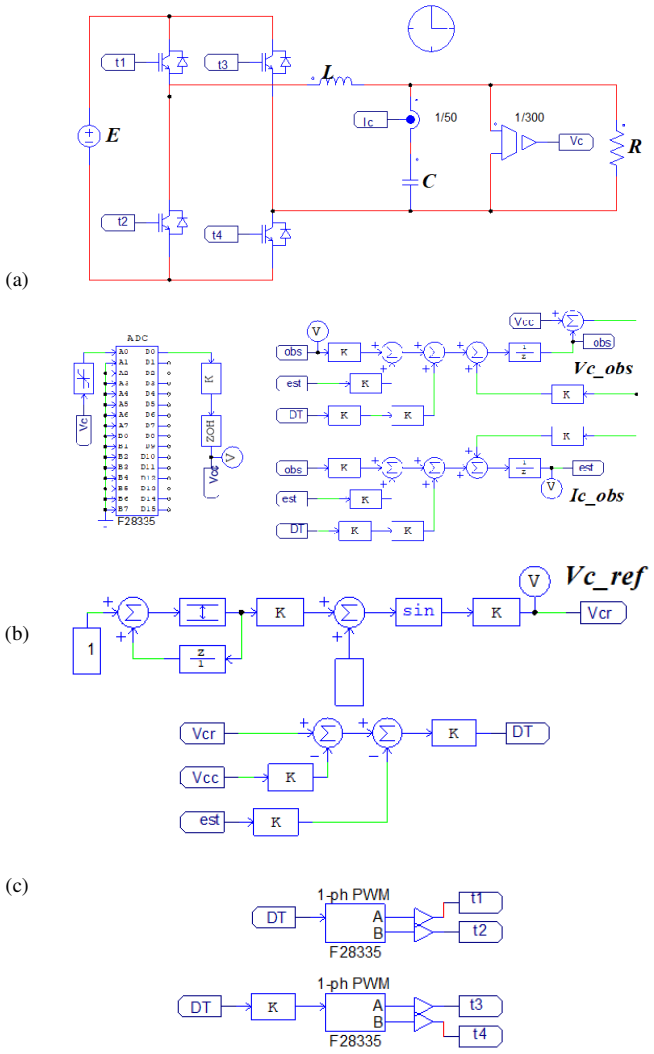


Fig. 5. Simulation of a deadbeat control with a PSIM observer. (a) Lyanberger observatory, (b) reference tension, (c) dead-beat control.

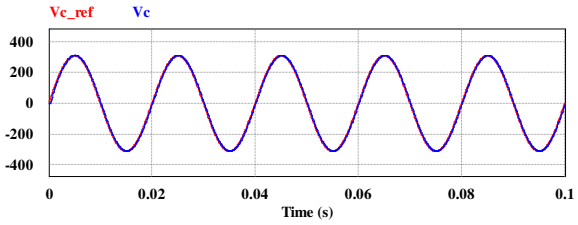


Fig. 6. Simulation result of the system without an observer.

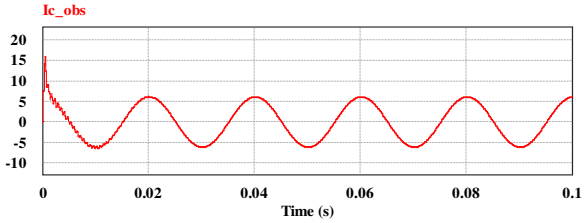


Fig. 7. Current observer of the capacitor.

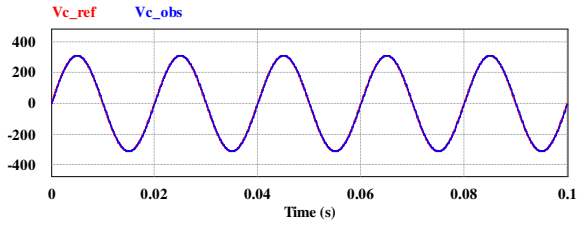


Fig. 8. Tension estimation with the reference tension.

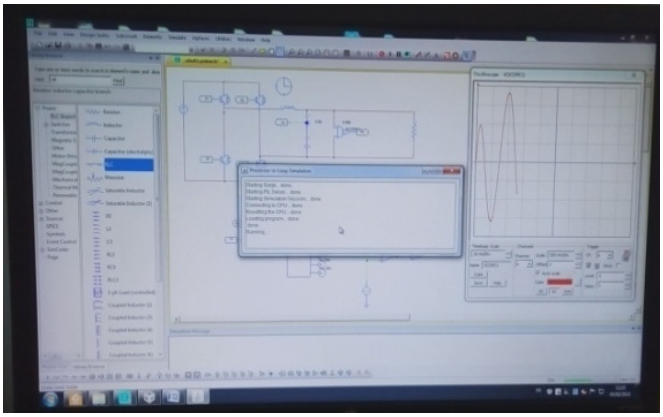
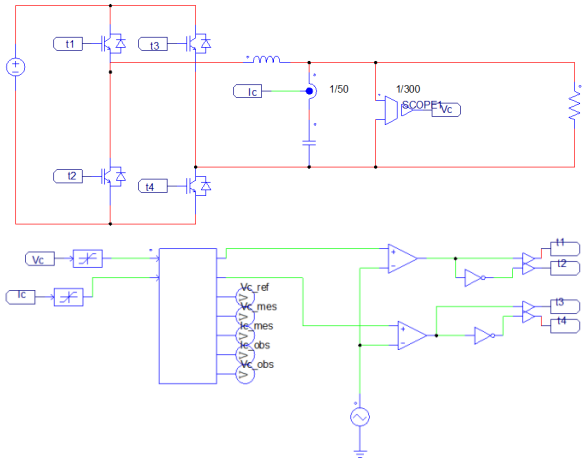


Fig. 9. PIL of dead-beat control whit observer.

Figure 10 shows a simulated block diagram with the PIL structure developed by PSIM in order to achieve safe and rapid prototyping. The control blocks (dead-beat) have been deleted and the creator code CCS has been added instead. This block uses the UART communication protocol to establish communication between the PSIM software and the FA28253. The inverter output voltage V_C values, which are input from the contact block, are supplied to the microcontroller at each step of the PSIM. The microcontroller gets the switching data (t_1, t_2, t_3, and t_4) of the inverter control, which is the output of the contact block. The cooperative effort between FA28253 and PSIM is built using this structure.

(a)



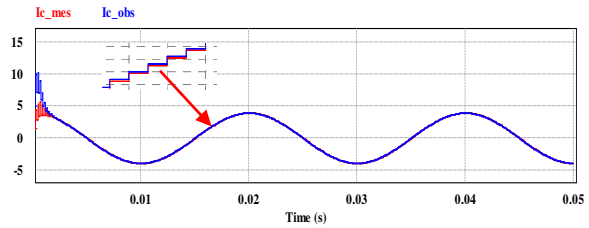
(b)

Fig. 10. PIL simulation of deadbeat control whit observer.

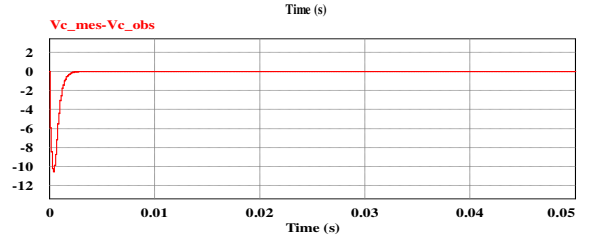
A. *Linear Load with R=20Ω*

Figure 11 shows the simulation result of the deadbeat control with linear load equal to 20Ω. A current sensor and the observer's current are used to show the effect of load variation, nonlinear load, and purely inductive load on the controller. We start with preliminary tests to show the robustness of the linear overload command. Purely sinusoidal current and voltage are applied, the current being phase shifted 90° ahead. The error of the current and voltage between the measurement system and the estimation is close to zero, the feedback fault of the measured voltage is controlled by the observer and is injected in the current observer.

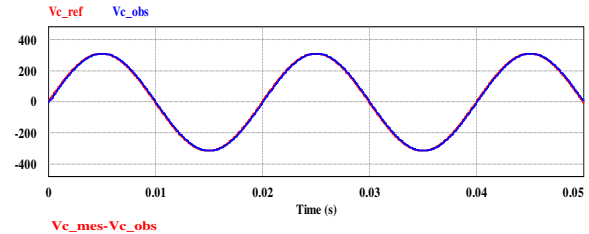
(a)



(b)



(c)



(d)

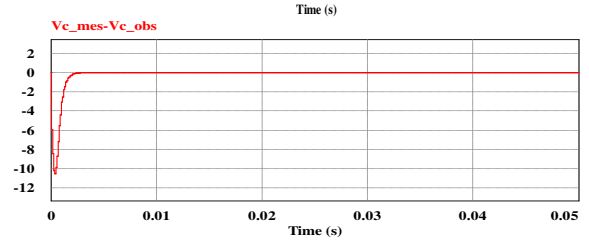


Fig. 11. PIL simulation of dead-beat control with observer: (a) current i_c (measured and observed), (b) error current, (c) voltage V_C (reference and observed), (d) voltage error.

B. *Linear Load R=20Ω with Increasing Load Up to 100%*

The PIL simulation of dead-beat control with increasing load up to 100% is presented in Figure 12. According to the obtained results, Figure 12 shows the PIL results for output voltage and current under a resistive load, at t = 0.045s. When the load is increased to 100%, we observe a voltage loss, which the control quickly recovers. In addition, the current is controlled relatively well, so it can be concluded that the controller is good.

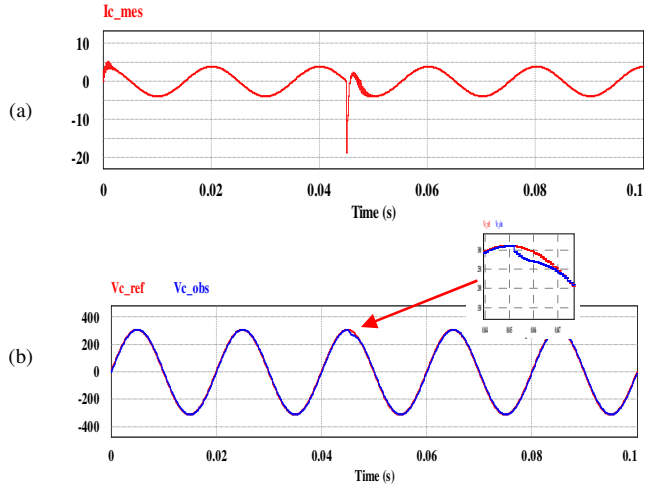


Fig. 12. PIL simulation of dead-beat control with increasing load up to 100%, equal to R=40Ω: (a) current i_C (measured and observed), (b) voltage V_C (reference and observed).

C. Nonlinear Load Diode Bridge with R=20Ω and C=30μF in Parallel

The proposed controller was then tested using a distorting load (a diode bridge with a capacitive filter of 30μF and a resistive load of 20Ω). The output voltage remains sinusoidal, but the capacitor current waveform deviates from the ideal sinusoidal waveform, as seen in Figure 13.

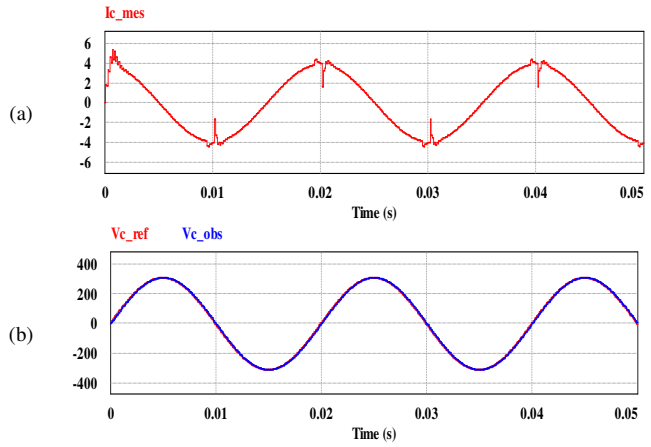


Fig. 13. PIL simulation of dead-beat control with nonlinear load diode bridge with R=20Ω and C=30uF on parallel: (a) current i_C (measured and observed), (b) voltage V_C (reference and observed).

According to the obtained results, the sudden connection of a nonlinear load has caused a distortion in the output current. However, the proposed controller has eliminated this distortion in the voltage.

D. Purely Inductive Load L=0.10H

Figure 14 presents the PIL simulation of dead-beat control with purely inductive load of L=0.10H. Figure 14 shows the PIL results for the output voltage and current for a purely inductive load.

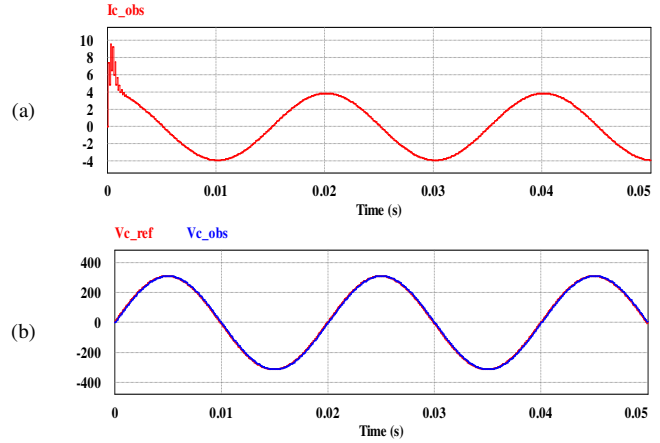


Fig. 14. PIL simulation of dead-beat control with purely inductive load L=0.10H: (a) current i_C (measured and observed), (b) voltage V_C (reference and observed).

We observe a voltage loss, which the control quickly recovers, but the capacitor current waveform deviates from the ideal sinusoidal waveform.

VII. CONCLUSION

In this work, a dead-beat control scheme for a single-phase inverter with an observer is described. The feasibility of the proposed controller with an observer has been demonstrated by simulations and was implemented in a processor in the PIL loop. The results showed that the proposed scheme achieves good voltage regulation with linear and nonlinear loads. The proposed controller does not have any parameters that can be changed, it needs a model of the system to calculate the controlled variables, allowing fast dynamic response of voltage control. It has been proved that the use of an observer allows a better estimation of the unknown capacitor current.

Dead-beat control serves a different approach for the control of power converters, considering the discrete nature of the converters and the microprocessors used for control. Moreover, the high calculation power of the current existing DSPs makes this method very attractive for controlling power converters.

Since the dead-beat controlled system's efficiency is successfully proved, the next steps are to study the dead-beat control of a grid-connected inverter, the islanded operation of an inverter, and the application of the proposed control to other inverter structures.

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